THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 17

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte ERIC W. SCHIEVE

Appeal No. 96-3850
Application No. 08/253,480[1]

ON BRIEF

Before THOMAS, HAIRSTON, and GROSS, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1 through 12, which are all of the claims pending in this application.

The appellant's invention relates to a system for testing hardware interrupt service routines for a microprocessor prior

[1] Application for patent filed June 3, 1994.

to the completion of the microprocessor's power-on self-test program. The system uses a diagnostic interrupt vector table set in a read/writable memory formed on the same semiconductor chip as the microprocessor. Claim 1 is illustrative of the claimed invention, and reads as follows:

> 1. A system for testing a plurality of hardware interrupt service routines for a microprocessor prior to the completion of a power-on, self-test (POST) program for the microprocessor, set in a read-only memory (ROM) of the microprocessor, the system incorporating a read/writable memory formed in the same semiconductor chip as the microprocessor and ordinarily inoperative during the POST, the system comprising:
>
> (a) a diagnostic interrupt vector table set in the read/writable memory, the table comprising a plurality of interrupt vectors corresponding to a plurality of hardware interrupt routines, and a physical address for each of the interrupt vectors corresponding to the address of a diagnostic interrupt service routine for that interrupt vector;
>
> (b) means for selecting one of a plurality of devices and for causing the selected device to initiate an interrupt signal;
>
> (c) circuitry for transmitting the interrupt signal to the microprocessor for recognition and storage of the interrupt signal;
>
> (d) means for accessing the read/writable memory for the interrupt signal and reading out the corresponding physical address; and
>
> (e) means for performing the diagnostic interrupt service routine.

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Treu	5,245,615	Sep. 14, 1993
Sato et al. (Sato)	5,291,585	Mar. 01, 1994

New prior art:

Siewiorek, D.P., et al., "Computer Structures: Principles and Examples", McGraw-Hill Publishing Company, NY (1982). (Siewiorek)

Claims 1 through 12 stand rejected under 35 U.S.C. § 103 as being unpatentable over Treu in view of Sato.

Reference is made to the examiner's answer (Paper No. 14, mailed April 3, 1996) for the examiner's complete reasoning in support of the rejections, and to the appellant's brief (Paper No. 13, filed January 30, 1996) and reply brief (Paper No. 15, filed June 3, 1996) for the appellant's arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated

by the appellant and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1 through 12.

Claim 1 recites:

> . . . a read/writable memory formed in the same semiconductor chip as the microprocessor and ordinarily inoperative during the POST, the system comprising:
> (a) a diagnostic interrupt vector table set in the read/writable memory. (underlining added for emphasis)

In other words the interrupt vector table set must be located in a memory that is 1)read/writable, 2)on the same semiconductor chip as the microprocessor, and 3)ordinarily inoperative during the POST.

The examiner admits in the rejection (Final Rejection, page 2) that with respect to Treu, "[n]ot explicitly taught is the use of an interrupt vector table." The examiner states (Answer, page 3), "Sato was cited as teaching an interrupt vector table being set in a read/writable memory." However, as pointed out by appellant (Brief, page 8), Sato "does not store the table in a memory formed on the same semiconductor chip as the microprocessor." The examiner attempts to overcome this deficiency by citing Siewiorek to illustrate

that the trend in microcomputers is to place more elements on the same semiconductor chip. Accordingly, he concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to place a memory on the same semiconductor chip as the microprocessor.

Although we agree that merely placing a memory on the same semiconductor chip as the microprocessor would have been obvious in light of the trends in microcomputers, the examiner has not indicated why it would have been obvious to an artisan to place in such a read/writable memory, the interrupt vector table. Furthermore, none of the references teach or suggest setting the diagnostic interrupt vector table in a read/writable memory that not only is formed in the same semiconductor chip as the microprocessor but also is ordinarily inoperative during a POST.

The examiner states (Answer, page 3), "As per Appellant's point that the read/writable memory is not normally available to the POST. The Examiner views the exclusive used [sic] of a memory, which was off-chip and has now been added on-chip for the same purpose, as neither novel or unobvious." The test for obviousness, however, is not how the examiner "views" the

combination, but rather whether or not there is some reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley, 837 F.2d 1044, 1052, 5 USPQ2d 1434, 1439 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hospital Systems, Inc. v. Montefiore Hospital, 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984); In re Sernaker, 702 F.2d 989, 994, 217 USPQ 1, 5 (Fed. Cir. 1983). Since the examiner has provided no prior art that teaches "a read/writable memory formed in the same semiconductor chip as the microprocessor and ordinarily inoperative during the POST," with "a diagnostic interrupt vector table set in the read/writable memory," (underlining added for emphasis) the examiner has failed to set forth a prima facie case of obviousness.

As to the method claims, independent claim 7 requires loading with interrupt vectors a read/writable memory formed on the same semiconductor chip as the microprocessor. As discussed above, the prior art falls short of teaching forming the particular read/writable memory with the interrupt vectors on the same semiconductor chip as the microprocessor. Accordingly, we cannot sustain the rejection.

CONCLUSION

The decision of the examiner to reject claims 1 through 12 under 35 U.S.C. § 103 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)
KENNETH W. HAIRSTON Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
ANITA PELLMAN GROSS Administrative Patent Judge	)

vsh

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